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Summary of The Previous Restriction

Restriction to one of the following inventions was previously required under 35 U.S.C.

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- I. Claims 1-17, and 57-59, drawn to a system with a scrub logic, classified in class 714, subclass 702.
- II. Claims 18-51, and 63, drawn to testing a system with fault management, classified in class 714, subclass 723.
- III. Claims 52-56 and 60-62, drawn to a testing method and software to perform the method, classified in class 714, subclass 710.

In response to the Restriction Requirement, Applicant elected, with traverse, to prosecute Invention I, claims 1-17, and 57-59. In response to Applicant's arguments concerning Groups I & II, the restriction was removed, leaving all claims currently pending for examination.

In the present Office Action, all claims 1-63 have been examined. However, Applicant did not traverse the restriction of claims 60-62. Applicant assumes that claims 60-62 were not intended to be re-instated by the Examiner and claim 60-62 remain withdrawn in the present response. Applicant respectfully requests that the Examiner confirm and/or clarify the status of the previously restricted claims.

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Remarks

This Amendment is responsive to the **May 31, 2006 Office Action**. Reexamination and reconsideration of claims 1-18 and 21-59 is respectfully requested.

Summary of The Office Action

Claims 15, 31, 48, and 49 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These claims have been amended.

Claims 1, 2, 4, 6-9, 11-15, 18, 19, 21-26, 28-32, 34, 35, 37, 39-42, 44-49, and 52-63 were rejected under 35 U.S.C. §102(e) as being anticipated by Larson et al. (U.S. Patent No. 6,832,340). Larson does not teach each and every element found in the claims and thus all the 35 U.S.C. §102(e) rejections should be withdrawn.

Claims 3, 5, 10, 16, 17, 20, 27, 33, 36, 38, 43, 50, and 51 were rejected under 35 U.S.C. §103(a) as being unpatentable over Larson. Larson does not qualify as a 35 U.S.C. §103(a) reference. Larson is disqualified under 35 U.S.C. §103(c) since it only qualifies as potential prior art under 35 U.S.C. §102(e) and yet was subject to an obligation of assignment to the same entity as the invention at the time the invention was made. Thus, all the 35 U.S.C. §103(a) rejections should be withdrawn. See, MPEP 706.02(I)(1).

The Amendment

Due to the previous amendment to claim 18, dependent claims 19 and 20 are now cancelled since their subject matter is covered by claims 2 and 3.

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The Claims Patentably Distinguish Over the References of Record

35 U.S.C. §102

For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach every element of the claim. Section 2133 of the MPEP recites:

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Larson

Larson describes a "4 + 1" RAID (redundant array of inexpensive disks) system that performs reactive memory error detecting and correcting. In Larson, during a read, a memory value is read from main memory to a cache memory as part of the read. The value is then checked. Testing of the location from which the value is read appears not to occur. Conversely, the invention concerns proactive memory error detecting and correcting after mirroring and redirecting. Larson does not describe a pro-active detecting and correcting system that performs mirroring and then memory scrubbing. In Larson, while satisfying a read to regular (e.g., non-mirrored) memory, if an error is detected then a scrub command may be induced through the memory controller. The scrub command will recreate corrected data and rewrite that corrected data into the memory system. If a write to the memory location occurs before the scrub command occurs, then the scrub may be cancelled. This appears to be an ad-hoc, check on read application, not the systematic approach claimed. The claimed invention does not wait for a location to be read before checking, detecting, and correcting. Instead, the claimed invention mirrors a section of memory to a mirrored location and checks the mirrored locations. Reads and writes not associated with the detecting and correcting will interact with the mirroring section while the mirrored section is being scrubbed by detecting and correcting logics.

The reactive operation of the RAID system is described at col. 5, lines 33-35, which identify Larson as concerning a "READ function in which errors are detected and corrected while being delivered to an external source." The description continues at col. 6, lines 6-9, "if no errors are detected, the data is simply passed to the host controller and eventually to an output device. However, if a single-bit error is detected by a memory controller 48a-e, the data is corrected by the memory controller 48a-e". Note that the error was detected when memory was

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read from its original location, not from a special mirroring location. The hardware in Larson does not include the extra memory into which memory is mirrored.

Independent Claim 1

Claim 1 recites a memory access logic that includes a memory (e.g., mirroring location) that can store mirrored locations and that can accept memory access requests that are redirected to this mirroring location. The memory access logic also includes a scrub logic that will cause main memory to be mirrored to the mirroring location and that will selectively scrub the mirrored locations. Larson does not teach these elements and thus this claim is not anticipated. In particular, Larson does not teach the mirroring action performed by the scrub logic.

The Office Action asserts that col. 7, lines 25-30 describe these elements. These lines contain mention of neither a memory (e.g., mirroring location) nor a scrub logic that mirrors a main memory location. Phrase by phrase analysis of this section reveals the deficiency:

Phrase	Memory for mirroring disclosed?	Scrub logic to perform mirroring disclosed?
Similarly, if a multi-bit error is detected by the error detection and correction devices 54a-e,	No	No
that data is corrected through the RAID memory engine 60 for delivery to a requesting device (not shown) such as a disk drive	No	No
and the scrubbing control logic 62 is notified by the error detection and correction device 54a-e that a memory location should be scrubbed.	No	no

This passage indicates that Larson will detect and correct errors using a scrub logic. However, what is missing is the scrub logic that mirrors main memory to a mirroring location to facilitate checking the mirrored location while reads and writes are redirected to the mirroring location. For at least this reason this claim is not anticipated and is in condition for allowance.

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Dependent Claims 2-17, 20-33

These claims depend, directly and/or indirectly, from claim 1. Claim 1 has been shown to be not anticipated. Thus these claims are similarly not anticipated.

Claim 2

Claim 2 depends from claim 1. Claim 1 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 2 recites that the memory access logic comprises an ASIC. The Office Action asserts that col. 3, line 14 teaches a memory access logic comprising an ASIC. This line reads "generally, one or more ASICs are located within the host controller 13." Thus, this line simply indicates that a host controller may include an ASIC. What this line does not indicate is that a memory access logic like that described in claim 1 can be formed in an ASIC. Since Larson does not teach the claimed memory access logic, it follows that Larson also does not provide the further limitation of the memory access logic comprising an ASIC. Additionally, this interpretation establishes the host controller 13 as purportedly being the claimed system. This is internally inconsistent with other assertions made in the Office Action. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 4

Claim 4 depends from claim 1. Claim 1 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 4 recites that the system includes a second memory that stores configuration parameters. The Office Action asserts that col. 4, lines 3-5 teach the additional memory. This line reads "the second side of the DIMM 22 may be identical to the first side and may comprise nine additional DRAM devices (not shown)." This line simply describes a common dual inline memory module. It does not indicate that a second memory has been added to an access logic to store configuration parameters. Since Larson does not teach the claimed memory access logic, it follows that Larson also does not provide the further limitation of a memory to store configuration parameters. For this additional reason this claim is not anticipated and is in condition for allowance.

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Claim 6

Claim 6 depends from claim 4. Claim 4 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 6 recites that the second memory is writeable by an application located external to the memory access logic. The Office Action asserts that col. 3, lines 40-42 teach this limitation. This line reads "In addition, data may be sent to and from the I/O controller 19 for use by other systems or external devices." Thus, according to this passage, the "system" taught by Larson must be the I/O controller 19. However, in the rationale attached to claim 2, the host controller 13 was established as the system. This is internally inconsistent and improper. Using this construction, it becomes quite clear that I/O controller 19 contains none of the elements listed in claims 1, 4, or 6. This passage does not indicate that the second memory is writeable by an external application. Instead it merely shows that conventional memory can be sent to and from an I/O controller. Since Larson does not teach the claimed second memory, it follows that Larson also does not provide the further limitation of an external logic being able to write the second memory. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 7

Claim 7 depends from claim 4. Claim 4 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 7 recites that the second memory stores an on/off parameter, addresses, rates, log configuration parameters, and so on. The Office Action asserts that col. 7, lines 16-22 teach this limitation. This passage reads "However, at this point, the data residing in the memory sub-system 40 may still be corrupted. To rectify this problem, the data in the memory sub-system 40 is overwritten or "scrubbed." For every data word in which a single-bit error is detected and flagged by the memory controller 42, a request is sent from the memory controller 42 to the scrubbing control logic 62..." This passage is completely devoid of a description of parameters that may be stored in the second memory. Since Larson does not teach the claimed second memory, it follows that Larson also does not describe the type of parameters stored in the second memory. For this additional reason this claim is not anticipated and is in condition for allowance.

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Claim 8

Claim 8 depends from claim 7. Claim 7 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 8 recites that a log configuration parameter may store an entry point address for a logging process. The Office Action asserts that col. 7, lines 40-45 teach this limitation. This passage reads "The buffer 64 is used to store the corrected data and corresponding address location temporarily until such a time that the scrubbing process can be implemented. Once the scrubbing control logic 62 receives an indicator (flag) that a corrupted data word has been detected and should be corrected in the memory sub-system 40, a request is sent..." This passage mentions neither a log configuration parameter nor a logging process. Thus, it follows that it also does not mention storing an entry point address for a logging process in the missing configuration parameter. While an address of a memory location to be scrubbed may be stored, this is not the same as storing the address of a process for performing error logging. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 9

Claim 9 depends from claim 1. Claim 1 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 9 recites that the system includes a log configured to store a result value associated with scrubbing the main memory location. The Office Action asserts that col. 7, lines 20-23 teach the log. This line reads "For every data word in which a single-bit error is detected and flagged by the memory controller 42, a request is sent from the memory controller 42 to the scrubbing control logic 62..." While this passage describes flagging a word having a single-bit error, there is no mention of a log that stores the result of scrubbing a location. Presumably the flag would be used to signal a scrub logic to begin its operation. The claimed log is interested in the result of the scrub, not the initiation of the scrub. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 11

Claim 11 depends from claim 9. Claim 9 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 11 recites that the system includes a log that can be read by an application located external to the memory access logic. The Office

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Action asserts that col. 3, lines 19-22 teach this external readability. This line reads "Furthermore, the ASICs in the host controller may also contain logic specifying ordering rules, buffer allocation, specifying transaction type, and logic for receiving and delivering data." While this passage describes in general how an ASIC can receive and deliver data, it says nothing about a log like that claimed being read by an application. Like all the other rejections concerning the log, the reference simply does not describe logging the result of a scrub operation. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 12

Claim 12 depends from claim 1. Claim 1 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 12 recites that the scrub logic can selectively generate a signal when a main memory location being scrubbed exhibits a memory error. The Office Action asserts that col. 6, lines 23-25 teach this signal. This line reads "the error detection capabilities in the memory control devices 48a-e may be turned off or eliminated." This passage says nothing about a scrub logic generating a signal. It is unclear how the Office Action can assert that a passage that describes how a piece of hardware can be turned on or off anticipates a scrub logic generating a signal upon detecting a memory error in mirrored memory. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 13

Claim 13 depends from claim 1. Claim 1 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 13 recites that the scrub logic can initiate scrubbing main memory by sending a signal to an onboard memory testing logic. This limitation gets to the proactive nature of the invention as compared to the reactive nature of Larson. In Larson, a read is issued and while servicing the read a memory error may be detected. Here, the system doesn't wait for that kind of random access. Instead, the invention can set aside memory to be tested and then initiate testing of that memory. The Office Action asserts that col. 5, lines 41-45 teach this self-initiated testing. This line reads "while the operations have been logically separated for simplicity, it should be understood that the elements described in each

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Fig. may reside in the same device, here the host controller.” This passage says nothing about a scrub logic initiating scrubbing. It is unclear how the Office Action can assert that a passage that describes how a functions can be separate or combined anticipates a scrub logic initiating testing. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 14

Claim 14 depends from claim 1. Claim 1 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 14 recites that the scrub logic can be written by an application located external to the memory access logic. The Office Action asserts that col. 3, lines 19-22 teach this external readability. This line reads “Furthermore, the ASICs in the host controller may also contain logic specifying ordering rules, buffer allocation, specifying transaction type, and logic for receiving and delivering data.” While this passage describes in general how an ASIC can receive and deliver data, it says nothing about a scrub logic like that claimed being written by an application. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 15

Claim 15 depends from claim 1. Claim 1 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 15 recites that the scrub logic scrubs main memory transparently to operating system control. The Office Action asserts that col. 3, lines 10-15 teach this transparency. This line reads “The host controller 13 serves as an interface directing signals between the processors 11, cache accelerators 14, a memory control block 15 (which may be comprised of one or more memory control devices as discussed with reference to FIGS. 5 and 6), and an I/O controller 19. Generally, one or more ASICs are located within the host controller 13.” This passage says nothing about the transparency of a scrub logic to an operating system. In Larson, it is possible that a read associated with an operating system might be impacted by the described detecting and “4 + 1” RAID correcting scheme. For example, a READ directed at a memory location for which correction is underway may be delayed. The claimed invention would not generate the same delay because the memory location being read would have been mirrored before being tested. For this additional reason this claim is not anticipated and is in condition for allowance.

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Claim 18

Claim 18 depends from claim 1. Claim 1 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 18 recites that the system includes a fault management logic to process a memory fault associated with a main memory location that has been mirrored and that is being scrubbed. The Office Action asserts that col. 6, lines 18-22 teach this fault management logic. This line reads "Therefore, if an error is detected and corrected by the memory controller 48a-e, a message is sent from the memory controller 48a-e to the host controller 44 indicating that a memory cartridge 46a-e should be scrubbed, as discussed in more detail below." It is unclear which, if any, of the listed elements operates as a fault management logic. While the memory controller may detect an error, there is no mention of detecting a memory fault. The Applicant invites a pinpoint citation within this passage as to which element purportedly operates as the fault management logic.

Claim 21

Claim 21 depends from claim 18. Claim 18 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 21 recites that a second memory stores configuration parameters associated with fault management processing. The Office Action asserts that col. 3, lines 30-35 teach the additional memory. This line reads "Bytes in a cache line may comprise several variable values. Cache lines in the memory 16 are moved to a cache for use by the processors 11 when the processors 11 request data stored in that particular cache line." This line simply describes that cache lines may store values for variables. It does not indicate that a second memory has been added to the access logic to store configuration parameters for fault management processing. While the cache may be a "second memory", it is not used for storing configuration parameters that control how the main memory is checked but rather to store the data that will be tested. Since Larson does not teach the claimed memory access logic and post-mirroring detecting, correcting, and/or fault management processing, it follows that Larson also does not provide the further limitation of a memory to store configuration parameters that control the post-mirroring actions. For this additional reason this claim is not anticipated and is in condition for allowance.

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Claim 22

Claim 22 depends from claim 21. Claim 21 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 22 recites that the second memory may be a register(s). The Office Action asserts that col. 4, lines 8-10 teach the additional limitation of registers. This line reads "System memory is generally accessed by CPUs and I/O devices as a cache line of data. A cache line generally comprises several 72-bit data words." This line simply describes the organization of a cache line. It says nothing about a second memory in a memory access logic being made from registers. While the cache may be a "second memory" in which data retrieved from main memory is stored, this memory is not described as being registers. Since Larson does not teach the claimed memory access logic and its second memory, it follows that Larson also does not provide the further limitation of the memory being implemented in registers. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 23

Claim 23 depends from claim 21. Claim 21 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 23 recites that the second memory may be writeable by an external application. The Office Action asserts that col. 3, lines 36-38 teach the additional limitation. Like almost all the other citations in the Office Action, this citation appears to have nothing to do with the additional limitation, leaving the limitation not taught by the reference. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 24

Claim 24 depends from claim 21. Claim 21 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 24 recites that the second memory stores an on/off parameter, addresses, rates, log configuration parameters, and so on. The Office Action asserts that col. 3, lines 42-44 teach this limitation. This passage reads "The I/O controller 19 may comprise a plurality of PCI-bridges, for example, and may include counters and timers as conventionally present in personal computer systems ..." This passage is completely off point, discussing I/O controller architecture rather than parameters that may be

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stored in a second memory in a memory access logic to control fault management processing. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 25

Claim 25 depends from claim 24. Claim 24 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 25 recites that a log configuration parameter may store an entry point address for a fault management process. The Office Action asserts that col. 7, lines 40-45 teach this limitation. This passage reads "The buffer 64 is used to store the corrected data and corresponding address location temporarily until such a time that the scrubbing process can be implemented. Once the scrubbing control logic 62 receives an indicator (flag) that a corrupted data word has been detected and should be corrected in the memory sub-system 40, a request is sent..." This passage mentions neither a log configuration parameter nor a fault management process. Thus, it follows that it also does not mention storing an entry point address for a fault management process in the missing configuration parameters. While an address of a memory location to be scrubbed may be stored, this is not the same as storing the address of a process for performing fault management. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 26

Claim 26 depends from claim 18. Claim 18 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 26 recites that the system includes a log configured to store a result value associated with fault management processing of a memory fault experienced by the main memory location during post mirroring fault management processing. The Office Action asserts that col. 7, lines 43-47 teach the log and the processing. This line reads "Once the scrubbing control logic 62 receives an indicator (flag) that a corrupted data word has been detected and should be corrected in the memory sub-system 40, a request is sent to an arbiter 66 which schedules and facilitates all accesses in the memory sub-system 40." While this passage describes processing a flag, there is no mention of a log that stores the result of memory fault processing. Presumably the flag would be used to signal a logic to begin its operation. However, the claimed log is interested in the result of memory fault processing, not

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its initiation. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 28

Claim 28 depends from claim 26. Claim 26 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 28 recites that the log that can be read by an application located external to the memory access logic. The Office Action asserts that col. 7, lines 43-47 teach this external readability. This line reads "Once the scrubbing control logic 62 receives an indicator (flag) that a corrupted data word has been detected and should be corrected in the memory sub-system 40, a request is sent to an arbiter 66 which schedules and facilitates all accesses in the memory sub-system 40." This passage describes in general how a scrubbing control logic may receive an indication that an error was detected. Like all the other rejections concerning the log, the reference simply does not describe logging the result of an operation, let alone having that log be readable by an application outside the memory access logic. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 29

Claim 29 depends from claim 18. Claim 18 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 29 recites that the fault management logic can selectively generate a signal when a main memory location exhibits a memory fault. The Office Action asserts that col. 7, lines 43-47 teach this signal. This line reads "Once the scrubbing control logic 62 receives an indicator (flag) that a corrupted data word has been detected and should be corrected in the memory sub-system 40, a request is sent to an arbiter 66 which schedules and facilitates all accesses in the memory sub-system 40." While this passage describes providing a scrubbing control logic with an indicator, it says nothing about a fault management logic generating a signal. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 30

Claim 30 depends from claim 18. Claim 18 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 30 recites that the fault management

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logic can be written by an application located external to the memory access logic. The Office Action asserts that col. 7, lines 40-51 teach this external write limitation. However, this passage describes storing corrected data until a scrubbing process can be implemented. There is no fault management logic described in Larson, and thus it follows that there is also no description of how it can be written by an external application. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 31

Claim 31 depends from claim 18. Claim 18 has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 31 recites that the fault management logic performs fault management transparently to operating system control. The Office Action asserts that col. 3, lines 10-15 teach this transparency. This line reads "The host controller 13 serves as an interface directing signals between the processors 11, cache accelerators 14, a memory control block 15 (which may be comprised of one or more memory control devices as discussed with reference to FIGS. 5 and 6), and an I/O controller 19. Generally, one or more ASICs are located within the host controller 13." This passage says nothing about the transparency of fault management processing to an operating system. In Larson, it is possible that a read associated with an operating system might be impacted by the described detecting and "4 + 1" RAID correcting scheme. For example, a READ directed at a memory location for which correction is underway may be delayed. The claimed invention would not suffer the same impact, because the memory location being read would have been mirrored. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 32

Claim 32 depends from claim 31. Claim 31 has been shown to be not anticipated. Thus this claim is similarly not anticipated. Additionally, this claim recites actions that the fault management logic may take, including logging data, correcting a fault, logically removing a location from main memory, and halting a computer. The Office Action asserts that Col. 7, lines 40-51 teach this limitation. Since the reference does not even teach a fault management logic, it follows that none of the actions described in this claim are taught by this passage. The Applicant invites a pinpoint citation in the passage, or elsewhere in the reference, where the fault

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management logic and/or the actions performed by the fault management logic as claimed in claim 32 are described.

Independent Claim 34

Claim 34 describes a main memory controller that can be connected to both a main memory and a processor. The claimed main memory controller includes a memory that can logically replace main memory locations. The claimed main memory controller also includes a scrub logic and a fault management logic. The scrub logic can scrub main memory locations and the fault management logic can process memory faults generated by the main memory locations. Both the scrub logic and fault management logic are claimed as being part of the main memory controller.

The Office Action asserts that this controller and its elements are described in Col. 6, lines 40-50. A phrase by phrase analysis of this passage reveals that none of these elements are described.

Phrase	Main Memory Controller With Scrub Logic?	Main Memory Controller With Fault Management Logic?
The memory controller 48a-e, with standard ECC capabilities, can detect the errors but will not be able to correct the data error.	No	No
Therefore, the erroneous data is passed to the error detection and correction devices 54a-e.	No	No
The error detection and correction devices 54a-e which also have typical ECC detection can detect the multi-bit errors and deliver the data to the RAID memory engine 60, via the READ/WRITE control logic 56, for correction.	No	No
The error detection and correction device 54a-e will also send a message to the scrubbing control logic 62 indicating that the memory cartridge 46a-e in which the	No	No

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erroneous data word originated should be scrubbed.		
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In fact, close review of these phrases indicates that a collaboration between many pieces is occurring and that no single memory controller includes all the claimed elements. For at least this reason this claim is not anticipated and is in condition for allowance.

Claim 35

Claim 35 depends from claim 34. Claim 34 has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, claim 35 recites that the main memory controller comprises an ASIC. While the reference describes a computer in which ASICs may appear, it does not describe the claimed main memory controller comprising an ASIC. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 37

Claim 37 depends from claim 34. Claim 34 has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, claim 37 recites that the main memory controller includes a second memory to store configuration parameters. While the reference describes a computer that may have a two level memory architecture (e.g., main memory, cache memory), it does not describe the "second memory" being used to store parameters that control how the main memory will be tested. Instead, the reference describes the cache memory being used only to store values retrieved from the main memory. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 39

Claim 39 was rejected using the same rationale as claim 11. The same arguments therefore apply and thus this claim has been shown to be not anticipated.

Claim 40

Claim 40 depends from 37, which has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 40 recites various values that the second memory may store. Since the reference does not even describe the second memory, it follows

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that it does not describe the additional limitations concerning the values that can be stored in the second memory. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 41

This claim was rejected using the same rationale as applied to claim 25. The same arguments therefore apply and thus this claim has been shown to be not anticipated.

Claim 42

Claim 42 depends from 34, which has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, claim 42 recites that the system includes a log that stores a result value associated with scrubbing or processing a memory fault. Since the reference does not even describe the mirroring then scrubbing and/or memory fault management processing, it follows that it does not describe the additional limitations concerning the values associated with these actions that can be stored. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 44

This claim was rejected using the same rationale as applied to claim 28. The same arguments therefore apply and thus this claim has been shown to be not anticipated.

Claim 45

This claim was rejected using the same rationale as applied to claim 13. The same arguments therefore apply and thus this claim has been shown to be not anticipated.

Claim 46

Claim 46 was rejected using the same rationale as claim 11. The same arguments therefore apply and claim 46 has been shown to be not anticipated.

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Claim 47

This claim was rejected using the same rationale as applied to claim 30. The same arguments therefore apply and thus this claim has been shown to be not anticipated.

Claim 48

This claim was rejected using the same rationale as applied to claim 15. The same arguments therefore apply and thus this claim has been shown to be not anticipated.

Claim 49

This claim was rejected using the same rationale as applied to claim 15. The same arguments therefore apply and thus this claim has been shown to be not anticipated.

Independent Claim 52

This claim was rejected using the same rationale as applied to claim 32. This is improper since claim 32 is a system claim and claim 52 is a method claim that includes its own distinct elements and limitations. For example, claim 52 describes selectively copying contents of a main memory location to a cache memory location in a main memory controller chipset. This may be referred to as "mirroring" the main memory location to a "mirroring" location. After this mirroring, there will be two locations storing the same values. Thus, the original location may be "logically replaced" by the mirroring location, which allows reads/writes to go to the mirroring location leaving the original location free to be tested and scrubbed. Thus, the method in claim 52 describes testing the original location(s) using a testing logic that exists in the main memory controller chipset.

The Office Action asserts that col. 7, lines 40-51 teach this method. However, this passage, and indeed the entire reference, is silent concerning the mirroring and then testing described in claim 52. While the reference describes a value being read into a cache from main memory, this is done as part of a read operation. The main memory remains logically coupled to and the direct target of the rest of the system. No portion of the main memory is logically removed as a target from the rest of the system. For at least this reason this claim is not anticipated and is in condition for allowance.

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Claim 53

This claim depends from claim 52. Claim 52 has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, claim 53 recites selectively processing memory faults that occur during the testing. Since the reference does not teach the method that tests after mirroring, it follows that it also does not teach this additional action. For this additional reason the claim is not anticipated and is in condition for allowance.

Claim 54

This claim depends from claim 53. Claim 53 has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, claim 54 further limits the actions that fault management processing may include. Since the reference does not teach that the method performs fault management processing after mirroring, it follows that it also does not teach these additional limitations. For this additional reason the claim is not anticipated and is in condition for allowance.

Claim 55

This claim depends from claim 52. Claim 52 has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, claim 55 recites different approaches for scrubbing memory (e.g., a striping test). Since the reference does not teach the method that tests after mirroring, it follows that it also does not teach these additional limitations. While the reference describes scrubbing using a parity test and a write back action, these actions are performed as the result of a read being presented to memory. They are not performed as the result of a dedicated test that is performed after a location has been mirrored. For this additional reason the claim is not anticipated and is in condition for allowance.

Independent Claim 56

Claim 56 claims a computer-readable medium that stores executable instructions for performing a method. The reference describes neither this computer-readable medium nor the method stored thereon. The Office Action recites the abstract, which describes a read and react RAID "4+1" system. The claimed invention is a proactive method stored on a computer readable medium. The method mirrors a first main memory location(s) to a second location(s),

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and then tests the first location(s). The reference does not do the mirroring first. The reads that cause the read and detect operations are performed against the equivalent of the second memory location, not the first (e.g., original) memory location. For at least this reason this claim is not anticipated and is in condition for allowance.

Claim 57

Claim 57 claims a memory access system that includes elements for mirroring, redirecting, and performing memory management operations on the mirrored location. The Office Action again just recites the abstract, which describes a read and react RAID "4+1" system. The claimed invention is a proactive system that mirrors a first main memory location(s) to a second location(s), redirects operations to the second location, and then performs operations on the first location(s). The reference does not do the mirroring first. The reads that cause the read and detect operations are performed against the equivalent of the second memory locations. For at least this reason this claim is not anticipated and is in condition for allowance.

Claim 58, Claim 59

These two claims were both rejected based on the Abstract. Both these claims depend from claim 57, which has been shown to be not anticipated. Additionally, these claims provide limitations on the memory management operations that are performed after mirroring and redirection. Since the reference describes neither mirroring nor redirection, it follows that it also does not describe these actions that can be performed after mirroring and redirection. For this additional reason these claims are not anticipated and are in condition for allowance.

Claims 60-62

These claims remain withdrawn. Applicant requests that the Examiner confirm the status of these claims.

Independent Claim 63

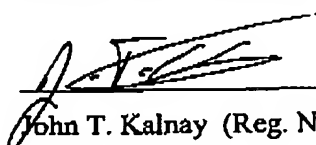
In view of the explanations of Larson, Applicant respectfully submits that Larson fails to anticipate each and every element of claim 63. Therefore, claim 63 patentably distinguishes over Larson and should be allowed.

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Conclusion

For the reasons set forth above, claims 1-18, 21-59 and 63 patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,



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